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EXAMINER	
GOLDBERG, BRIAN J	

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2861	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,808	WADE ET AL.	
	Examiner	Art Unit	
	Brian Goldberg	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/04, 6/3/04, 6/8/04, 6/27/05*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 9-35, 39, 41, and 42 are objected to because of the following informalities:

2. Regarding claim 2, "thin-flim" should be "thin-film" in line 2 of the claim.

3. Regarding claim 9, "after the second set of N memory elements receives the third set of N memory elements is configured to serially receive..." is not proper and it is unclear what is meant.

4. Regarding claim 10, the word "the" should be deleted from "wherein the each" in the first line of the claim. Also, claim 10 recites the limitation "the clock" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

5. Regarding claim 13, a space needs to be added between "enablingvalues" in line 3 of the claim.

6. Claim 15 recites the limitations "the corresponding fire enable shift register memory element" in line 4 of the claim, "the corresponding memory element" in line 5 of the claim, "the hold shift register" in lines 5-6 of the claim, "the switch control signal" in line 11 of the claim, and "the first state" in the last line of the claim. There is insufficient antecedent basis for these limitations in the claim.

7. Regarding claim 18, the word "of" should be added between "series values" in lines 1-2 of the claim. Also, claim 18 recites the limitations "the corresponding memory element" in line 7 of the claim, "the corresponding value" in line 8 of the claim, and "the

at least one enable state" in lines 8-9 of the claim. There is insufficient antecedent basis for these limitations in the claim.

8. Claim 22 recites the limitation "the set of N memory elements" and it is unclear to which set the claim refers.

9. Claim 24 recites the limitation "the fire enable value" in lines 5-6 of the claim. There is insufficient antecedent basis for this limitation in the claim.

10. Regarding claim 27, the last word of the claim should be "state", not "sate". Also, claim 27 recites the limitation "the enable state" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

11. Regarding claim 31, the word "cycle" should be "cycles" in the line 4 of the claim. Also, claim 31 recites the limitation "the disable state" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

12. Regarding claim 32, "an logic" should be "a logic" in line 3 of the claim.

13. Regarding claim 33, "and AND-gate" should be "an AND-gate" in line 2 of the claim.

14. Regarding claim 39, the word "of" should be added between plurality and memory in line 2 of the claim and the claim should not end with ";". Also, claim 39 recites the limitation "the value" in line 7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

15. Regarding claim 41, "wherein N of the plurality of fluid ejecting elements into a plurality of zones" is not proper and it is unclear what is meant.

16. Claim 42 recites the limitation "the fire enable value" in line 9 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

17. Claims 1, 4, 5, 10-12, 15-18, 20, 21, 22, 24-30, and 32-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Saunders et al. (US 5541629).

18. Regarding claim 1, Saunders et al. disclose "a first set of N memory elements (40 of Fig 8) each storing a fire enable value (PE of Fig 8), each of the N memory elements configured to be updated; and N fluid ejecting elements (31 of Fig 3), each fluid ejecting element corresponding to a different one of the N memory elements (see Fig 3) and configured to receive the fire enable value from the corresponding memory element, wherein the fluid ejecting element is enabled to eject a fluid when the fire enable value is an enabling value (col 5 ln 5-21)."

19. Regarding claim 4, Saunders et al. disclose "a second set of N memory elements (34 of Fig 8), each memory element storing a different one of N sub-blocks of an image data block, wherein each sub-block of image data includes an enabling value and a disabling value (col 4 ln 47-61)."

20. Regarding claim 5, Saunders et al. disclose "wherein the image data block comprises a row of image data and each sub-block comprises a bit of image data (col 6 ln 49-50)."

21. Regarding claim 10, Saunders et al. disclose "each of the N fluid ejecting elements (31, 32 of Fig 3) corresponds to a different one of the N memory elements (34, 36 of Fig 7) of the second set of N memory elements and is configured to receive upon each cycle of the clock (37 of Fig 6) the image data sub-block from the corresponding memory element, wherein the fluid ejecting element generates an ink droplet when the fire enable value is the enabling value and when the image data sub-block is the enabling value (col 5 ln 34-45)."

22. Regarding claim 11, Saunders et al. disclose "the fluid ejecting element does not generate an ink droplet when one of the fire enable value or the image data sub-block is the disabling value (col 5 ln 34-45)."

23. Regarding claim 12, Saunders et al. disclose "the N fluid ejecting elements (31 of Fig 3) are configured to print a block of image data in a print cycle, and wherein the first set of N memory elements (40 of Fig 8) is configured to serially receive in the print cycle a series of fire enable values representative of a fire enable pulse, wherein the first set of N memory elements receives a fire enable value (PE of Fig 8) upon each cycle of the clock (37 of Fig 7), with a first fire enable value of the series being received upon a first clock cycle of the print cycle and a last fire enable value of the series being received upon a last clock cycle of the print cycle (col 5 ln 34-45)."

24. Regarding claim 15, Saunders et al. disclose "a logic element (48 of Fig 4A and Fig 5) configured to receive a fire enable value (PE of Fig 8) from the corresponding fire enable shift register memory element (40 of Fig 3) and to receive an image data sub-block from the corresponding memory element of the hold shift register, and to provide

a power switch control signal having a first state when the fire enable value and the image data sub-block each are the enabling value (col 5 ln 26-45); a heater resistor (44 of Fig 4A) having a first terminal connectable to a power source (24 of Fig 4A) and a second terminal; a switch (46 of Fig 4A) coupled between the second heater resistor terminal and ground (26 of Fig 4A) and receiving the switch control signal at control (48 of Fig 4A), and configured to connect the second terminal of the heater resistor to ground when the switch control signal has the first state (see Fig 4A)."

25. Regarding claim 16, Saunders et al. disclose "a field effect transistor (46 of Fig 4A) having a gate coupled to the logic element (48 of Fig 4A), a drain coupled to the second terminal of the heater resistor (44 of Fig 4A), and a source coupled to ground (26 of Fig 4A)."

26. Regarding claim 17, Saunders et al. disclose "an AND-gate (48 of Fig 4A) having a first input coupled to the corresponding memory element (40, PE of Fig 8) of the fire enable shift register, a second input coupled to the corresponding memory element (34, A of Fig 8) of the data hold shift register, and an output providing the power switch (46 of Fig 4A) control signal."

27. Regarding claim 18, Saunders et al. disclose "a series of N memory elements (40 of Fig 8) configured to serially receive a series values including at least one enabling value (PE of Fig 8) and to serially transfer the series of values through the series of N memory elements; and N fluid ejecting elements (31 of Fig 3), each fluid ejecting element coupled to a different one of the N memory elements and configured to receive the value from the corresponding memory element, wherein each fluid ejecting element

is enabled to eject a fluid when the corresponding value has the at least one enable state (col 5 ln 5-21)."

28. Regarding claim 20, Saunders et al. disclose "a first set of N memory elements (40 of Fig 8), each memory element of the first set storing one bit of image data of a row of image data, wherein each bit of image data is one of an enabling value or a disabling value (col 4 ln 47-61, col 6 ln 49-50)."

29. Regarding claim 21, Saunders et al. disclose "a second set of N memory elements (34 of Fig 8), each memory element storing one bit of image data of a row of image data, wherein each bit of image data is one of the enabling value or the disabling value (col 4 ln 47-61, col 6 ln 49-50)."

30. Regarding claim 22, Saunders et al. disclose "the set of N memory elements and the first and second set of N memory elements (34 and 40 of Fig 8) each comprise a shift register having N memory elements (36 of Fig 6, 42 of Fig 7)."

31. Regarding claim 24, Saunders et al. disclose "each of the N fluid ejecting elements (31 of Fig 3) corresponds to a different one of the N memory elements (42 of Fig 7) of the first set of N memory elements and is configured to receive upon each cycle of a clock (37 of Fig 7) the image data bit from the corresponding memory element, wherein the fluid ejecting element is configured to eject an ink droplet when the fire enable value is the enabling value and when the image data bit is the enabling value, and wherein the fluid ejecting element does not eject an ink droplet when either the fire enable value or the image data bit is the disabling value (col 5 ln 34-45)."

32. Regarding claim 25, Saunders et al. disclose "the N fluid ejecting elements (31 of Fig 3) are configured to print a row of image data in a print cycle (col 6 ln 49-50).

33. Regarding claim 26, Saunders et al. disclose "the series of N memory elements (32 of Fig 3) is configured to serially receive during the print cycle a fire enable pulse comprising a series of fire enable values (PE of Fig 8), wherein the series of N memory elements receives one fire enable value of the series upon each cycle of the clock (37 of Fig 7, col 5 ln 34-45).

34. Regarding claim 27, Saunders et al. disclose "storing a fire enable value (PE of Fig 8) in each of N memory elements (42 of Fig 7) of a fire enable shift register (40 of Fig 8), wherein each memory element corresponds to a different one of the N fluid ejecting elements (31 of Fig 3), each fire enable value being one of an enabling value or a disabling value (col 5 ln 5-21); updating the fire enable value in each of the N memory elements of the fire enable shift register from a fire enable value from an adjacent memory element upon each cycle of a clock (37 of Fig 7, col 5 ln 34-45); providing upon each cycle of the clock to each of the N fluid ejecting elements the fire enable value from the corresponding memory element for the fire enable shift register, wherein the fluid ejecting element is enabled to generate an ink drop when the fire enable value has the enable state (col 5 ln 5-21, ln 34-45)."

35. Regarding claim 28, Saunders et al. disclose "storing an image data value in each of N memory elements of an image data shift register, wherein each memory element corresponds to a different one of the N fluid ejecting elements, each image

data value being one of an enabling value or a disabling value (col 4 ln 47-61, col 5 ln 5-21)."

36. Regarding claim 29, Saunders et al. disclose "providing upon each cycle of the clock (37 of Fig 7) to each of the N fluid ejecting elements (31 of Fig 3) the image data value from the corresponding memory element, wherein the fluid ejecting element is configured to generate an ink drop when the fire enable value and the image data value are both enabling values (col 5 ln 5-21, ln 34-45)."

37. Regarding claim 30, Saunders et al. disclose "receiving serially in a print cycle at the fire enable shift register (40 of Fig 8) a series of fire enable values (PE of Fig 8) representative of a fire enable pulse, wherein the fire enable shift register receives a fire enable value upon each clock cycle (37 of Fig 7) of the print cycle with a first enable value of the series being received upon a first clock cycle of the print cycle and a last fire enable value of the series being received upon a last clock cycle of the print cycle (col 5 ln 34-45)."

38. Regarding claim 32, Saunders et al. disclose "a logic gate (48 of Fig 4A) having a first input terminal connectable to a corresponding memory element of a fire enable shift register (PEy of Fig 4A); a second input terminal connectable to a corresponding memory element of a data hold shift register (Ax of Fig 4A); and having an output terminal; a heating element (44 of Fig 4A) having first terminal connectable to a power source (24 of Fig 4A), and a second terminal; and a switch (46 of Fig 4A) coupled between the second terminal and ground (26 of Fig 4A), and having a control gate (48 of Fig 4A) coupled to the output terminal."

39. Regarding claim 33, Saunders et al. disclose "the logic gate comprises an AND-gate (col 5 ln 30-31)."

40. Regarding claim 34, Saunders et al. disclose "the heating element comprises a resistor (44 of Fig 4A, col 5 ln 27-28)."

41. Regarding claim 35, Saunders et al. disclose "the switch (46 of Fig 4A) comprises a field effect transistor having a gate coupled to the output terminal (col 5 ln 29-32)."

42. Regarding claim 36, Saunders et al. disclose "N fluid ejecting elements (31 of Fig 3); means for storing N fire enable values (40 of Fig 3) each corresponding to a different one of the N fluid ejecting elements and each being one of an enabling value or a disabling value (col 5 ln 5-21); and means for serially transferring each of the N fire enable values upon each cycle of a clock (37 of Fig 7, col 5 ln 34-45) and for providing to each of the N fluid ejecting elements upon each cycle of the clock the corresponding fire enable value from the storage means, wherein the fluid ejecting element is enabled to generate an ink drop when the fire enable value is an enabling value (col 5 ln 5-21, ln 34-45)."

43. Regarding claim 37, Saunders et al. disclose "means for storing N image data values each corresponding to a different one of the N fluid ejecting elements and each being one of an enabling value or a disabling value (col 4 ln 47-61, col 5 ln 5-21)."

44. Regarding claim 38, Saunders et al. disclose "N fire enable memory elements (42 of Fig 7) arranged into a plurality of zones (see Fig 7), each memory element storing a fire enable value (PE of Fig 8) being an enabling value; a fire enable controller (28, 30

of Fig 3) configured to individually control for each memory element zone a duration of how long each memory element stores the enabling value (col 4 ln 12-15); and N fluid ejecting elements (31 of Fig 3), each fluid ejecting element corresponding to a different one of the N memory elements and configured to receive the fire enable value from the corresponding memory element, wherein the fluid ejecting element is enabled to eject fluid when the fire enable value is the enabling value (col 5 ln 5-21, ln 34-45)."

45. Regarding claim 39, Saunders et al. disclose "a plurality of memory element sets (40 of Fig 3), each set having a plurality of memory elements (42 of Fig 7) such that a sum of the memory elements of the plurality of memory element sets equals N, with each memory element capable of storing an enabling value (PE of Fig 8); N fluid ejecting elements (31 of Fig 3), each fluid ejecting element corresponding to a different one of the N memory elements and configured to receive the value from the corresponding memory element, wherein the fluid ejecting element is enabled to eject fluid when the value is the enabling value (col 5 ln 5-21, ln 34-45); and a fire enable controller (28, 30 of Fig 3) individually controlling a duration that the enabling value is stored in the memory elements of each memory element set."

46. Regarding claim 40, Saunders et al. disclose "a first set of N memory elements (40 of Fig 8), each memory element configured to store a series of first values (PE of Fig 8); a second set of N memory elements (34 of Fig 8), each memory element configured to store a series of second values (A of Fig 8); N combiners (48 of Fig 4A), each having a first input coupled to a corresponding one of the memory elements of the first set of N memory elements (PEy of Fig 4A), a second input coupled to a

corresponding one of the memory elements of the second set of N memory elements (Ax of Fig 4A), and configured to provide a series of combined values including at least one enabling value based on the first and second values stored in the corresponding memory elements of the first and second set of N memory elements (col 5 ln 34-45); and N fluid ejecting elements (31 of Fig 3), each corresponding to and configured to receive the series of combined values from a corresponding one of the N combiners and enabled to eject fluid when the combined value is the enabling value (col 5 ln 5-21, ln 34-45)."

47. Regarding claim 41, Saunders et al. disclose "storing a value being one of an enabling value or a disabling value in each of N memory elements (42 of Fig 7), each memory element corresponding to a different one of the N fluid ejecting elements; and enabling each fluid ejecting element to eject fluid when the value stored in the corresponding memory element is an enabling value (col 5 ln 5-21); and controlling (28, 30 of Fig 3, 37 of Fig 7) individually for each zone a duration that an enabling value is stored in each corresponding memory element of the zone."

48. Regarding claim 42, Saunders et al. disclose "N fire enable memory elements (42 of Fig 7) arranged into a plurality of memory element zones, each memory element storing a value being one of an enabling value or a disabling value (col 5 ln 5-21); means for individually controlling a duration of the at least one enable state for each memory element zone (28, 30 of Fig 3, 37 of Fig 7); and means for providing a value from each of the N memory elements to a corresponding different one of N fluid ejecting

elements, wherein each fluid ejecting element is enabled to eject a fluid when the fire enable value is the enabling value (col 5 ln 5-21, 34-45).

49. Claims 1-4, 10-14, 18, 19, 27, 30, 31, and 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Anderson (US 6471320).

50. Regarding claim 1, Anderson discloses "a first set of N memory elements (102 of Fig 3) each storing a fire enable value (col 6 ln 58-62), each of the N memory elements configured to be updated; and N fluid ejecting elements (113 of Fig 3), each fluid ejecting element corresponding to a different one of the N memory elements (see Fig 3) and configured to receive the fire enable value from the corresponding memory element, wherein the fluid ejecting element is enabled to eject a fluid when the fire enable value is an enabling value (col 7 ln 43-45)."

51. Regarding claim 2, Anderson discloses "the first set of N memory elements and each of the N fluid ejecting elements are formed on a thin-film structure formed on a substrate including a non-conductive material selected from a group consisting of an oxide formed on a metal, a carbon composite material, a ceramic material, and glass see Fig 2 and col 6 ln 28-37)."

52. Regarding claim 3, Anderson discloses "the N fluid ejecting elements are configured as a row that extends substantially for a width of a page of print media (col 5 ln 60-62)."

53. Regarding claim 4, Anderson discloses "a second set of N memory elements (202 of Fig 3), each memory element storing a different one of N sub-blocks of an

image data block, wherein each sub-block of image data includes an enabling value and a disabling value (col 6 ln 58-62, col 7 ln 44-45)."

54. Regarding claim 10, Anderson discloses "each of the N fluid ejecting elements (113 of Fig 3) corresponds to a different one of the N memory elements (202 of Fig 3) of the second set of N memory elements and is configured to receive upon each cycle of the clock (52 of Fig 3) the image data sub-block from the corresponding memory element, wherein the fluid ejecting element generates an ink droplet when the fire enable value is the enabling value and when the image data sub-block is the enabling value (col 7 ln 43-45 and see Fig 3)."

55. Regarding claim 11, Anderson discloses "the fluid ejecting element does not generate an ink droplet when one of the fire enable value or the image data sub-block is the disabling value (col 7 ln 30-42)."

56. Regarding claim 12, Anderson discloses "the N fluid ejecting elements (113 of Fig 3) are configured to print a block of image data in a print cycle, and wherein the first set of N memory elements (102 of Fig 3) is configured to serially receive in the print cycle a series of fire enable values representative of a fire enable pulse, wherein the first set of N memory elements receives a fire enable value upon each cycle of the clock (52 of Fig 3), with a first fire enable value of the series being received upon a first clock cycle of the print cycle and a last fire enable value of the series being received upon a last clock cycle of the print cycle (col 7 ln 30-45, col 6 ln 62-65)."

57. Regarding claim 13, Anderson discloses "a first X fire enable values of the series received during a first X clock cycles of the print cycle are enabling values and a

remaining N fire enable values of the series received during a remaining N clock cycles of the print cycle are disabling values such that the enabling values propagate through the first set of N memory elements in a print cycle, wherein at an end of the print cycle each of the N memory elements of the first set of N memory elements is storing the disabling value (col 6 ln 67 – col 7 ln 9, col 7 ln 30-45)."

58. Regarding claim 14, Anderson discloses "a product of X multiplied by a duration of the clock cycle substantially equals an enable pulse duration (col 7 ln 36-40)."

59. Regarding claim 18, Anderson discloses "a series of N memory elements (102 of Fig 3) configured to serially receive a series values including at least one enabling value and to serially transfer the series of values through the series of N memory elements (col 6 ln 58-62, col 7 ln 8-9); and N fluid ejecting elements (113 of Fig 3), each fluid ejecting element coupled to a different one of the N memory elements and configured to receive the value from the corresponding memory element, wherein each fluid ejecting element is enabled to eject a fluid when the corresponding value has the at least one enable state (col 7 ln 43-45, see Fig 3).

60. Regarding claim 19, Anderson discloses "the series of N memory elements (102 of Fig 3) and each of the N fluid ejecting elements are formed on a thin-film structure formed on a substrate including a non-conductive material selected from a group consisting of an oxide formed on a metal, a carbon composite material, a ceramic material, and glass (see Fig 2, col 6 ln 28-37)."

61. Regarding claim 27, Anderson discloses "storing a fire enable value in each of N memory elements of a fire enable shift register (102 of Fig 3), wherein each memory

element corresponds to a different one of the N fluid ejecting elements (113 of Fig 3), each fire enable value being one of an enabling value or a disabling value (col 6 ln 58-62, col 7 ln 43-45); updating the fire enable value in each of the N memory elements of the fire enable shift register from a fire enable value from an adjacent memory element upon each cycle of a clock (52 of Fig 3); providing upon each cycle of the clock to each of the N fluid ejecting elements the fire enable value from the corresponding memory element for the fire enable shift register, wherein the fluid ejecting element is enabled to generate an ink drop when the fire enable value has the enable state (col 7 ln 43-45, see Fig 3)."

62. Regarding claim 30, Anderson discloses "receiving serially in a print cycle at the fire enable shift register a series of fire enable values representative of a fire enable pulse (col 6 ln 58-62), wherein the fire enable shift register receives a fire enable value upon each clock cycle (52 of Fig 3) of the print cycle with a first enable value of the series being received upon a first clock cycle of the print cycle and a last fire enable value of the series being received upon a last clock cycle of the print cycle (col 7 ln 30-45, col 6 ln 62-65).

63. Regarding claim 31, Anderson discloses "receiving a first X fire enable values of the series being enabling values during a first X clock cycles of the print cycle and a remaining N enable values of the series having the disable state during a remaining N clock cycle of the print cycle such that the first X fire enable values being enabling values propagate through the N memory elements of the fire enable shift register in a print cycle thereby sequentially enabling each of the N fluid ejecting elements to

generate an ink droplet for a duration substantially equal to a product of X multiplied by a duration of a clock cycle (col 6 ln 67 – col 7 ln 9, col 7 ln 30-45)."

64. Regarding claim 36, Anderson discloses "N fluid ejecting elements (113 of Fig 3); means for storing N fire enable values each corresponding to a different one of the N fluid ejecting elements and each being one of an enabling value or a disabling value (col 6 ln 58-62, col 7 ln 43-45); and means for serially transferring each of the N fire enable values upon each cycle of a clock (52 of Fig 3) and for providing to each of the N fluid ejecting elements upon each cycle of the clock the corresponding fire enable value from the storage means, wherein the fluid ejecting element is enabled to generate an ink drop when the fire enable value is an enabling value (col 7 ln 30-45, col 6 ln 62-65)."

Claim Rejections - 35 USC § 103

65. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

66. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. in view of *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960).

67. Regarding claims 6 and 7, Saunders et al. disclose the claimed invention as set forth above with respect to claim 5 as well as each set of N memory elements "comprise a shift register having N memory elements (34 and 40 of Fig 8)." Saunders et al. meet

the claimed invention except "a third set of N memory elements, each memory element storing a different one of N sub-blocks of an image data block, wherein each sub-block of image data includes an enabling value and a disabling value." *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960) addresses duplicating a part for a multiple effect. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to duplicate the set of memory elements set forth above by Saunders et al. in claim 4. One would have been motivated to so modify Saunders et al. for the benefit of making the memory more robust by allowing it to store more data.

68. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. in view of *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960) and further in view of Anderson. Saunders et al. in view of *In re Harza* disclose the claimed invention as set forth above with respect to claim 6. Thus Saunders et al. in view of *In re Harza* meet the claimed invention except "after the second set of N memory elements receives the third set of N memory elements is configured to serially receive and store N sub-blocks of a next image data block."

69. Anderson discloses "after the second set of N memory elements receives the third set of N memory elements is configured to serially receive and store N sub-blocks of a next image data block (col 8 ln 61-65, col 6 ln 66 - col 7 ln 1)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to serially receive and store N sub-blocks of a next image data block. One would have been motivated to so modify Saunders et al. in view of *In re Harza* for the benefit of streamlining the data transfer process by making it cyclical.

70. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. in view of *In re Harza*, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960) and further in view of Norton (US 6309040). Saunders et al. in view of *In re Harza* disclose the claimed invention as set forth above with respect to claim 6. Thus Saunders et al. in view of *In re Harza* meet the claimed invention except "the second set of N memory elements is configured to receive the image data block from the third set of N memory elements in response to a load enable signal."

71. Norton discloses "the second set of N memory elements is configured to receive the image data block from the third set of N memory elements in response to a load enable signal (206 of Fig 2, col 1 ln 45-47)." Norton discloses a load signal that transfers the image data contents of a shift register to another register. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to transfer image data from one set of memory elements to another set of memory elements in response to a load signal. One would have been motivated to so modify Saunders et al. in view of *In re Harza* for the benefit of more accurately controlling the transferring of data.

72. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. in view of Norton and further in view of Anderson.

73. Saunders et al. disclose the claimed invention as set forth above with respect to claim 22 as well as the first set of N memory elements (40 of Fig 8) corresponds to a different one of the N memory elements of the second set of N memory elements (34 of Fig 8)". Thus Saunders et al. meet the claimed invention except "wherein the first set of

N memory elements is configured to receive a present row of image data from the second set of N memory elements in response to a load enable signal, and wherein the second set of N memory elements is configured to serially receive a next row of image data after providing the present row of image data to the first set of N memory elements."

74. Norton discloses "wherein the first set of N memory elements is configured to receive a present row of image data from the second set of N memory elements in response to a load enable signal (206 of Fig 2, col 1 ln 45-47)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to transfer image data from one set of memory elements to another set of memory elements in response to a load signal. One would have been motivated to so modify Saunders et al. for the benefit of more accurately controlling the transferring of data.

75. Anderson discloses "wherein the second set of N memory elements is configured to serially receive a next row of image data after providing the present row of image data to the first set of N memory elements (col 8 ln 61-65, col 6 ln 66 - col 7 ln 1)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to serially receive and store a next row of image data. One would have been motivated to so modify Saunders et al. in view of Norton for the benefit of streamlining the data transfer process by making it cyclical.

76. Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saunders et al. in view of Norton.

77. Saunders et al. disclose "a shift register having a first set of memory elements (40 of Fig 8), each memory element storing a first enable value (PE of Fig 8) being one of an enabling value or a disabling value (col 5 ln 5-21); and a plurality of drop ejecting elements (31 of Fig 3), each drop ejecting element corresponding to and configured to receive the first enable value from a different one of the plurality of memory elements and each configured to receive a corresponding second enable value having an enable state (col 5 ln 5-21, ln 34-45), each drop ejecting element having a heating circuit (see Fig 4A) configured to: operate in a first mode to generate heat sufficient to cause the corresponding drop ejecting element to eject fluid (col 5 ln 27-45)" Thus Saunders et al. meet the claimed invention except the heating circuit being able to "operate in a second mode to generate heat sufficient to warm the corresponding drop ejecting element, but insufficient to cause fluid to be ejected."

78. Norton discloses "a second mode to generate heat sufficient to warm the corresponding drop ejecting element, but insufficient to cause fluid to be ejected (510 of Fig 5, col 5 ln 35-37, and the last line of the abstract)." It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to provide a second warming mode. One would have been motivated to so modify Saunders et al. for the benefit of maintaining acceptable print quality as stated by Norton in column 1 lines 29-30.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Goldberg whose telephone number is 571-272-2728. The examiner can normally be reached on Monday through Friday, 9AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Talbott can be reached on 571-272-1934. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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BJG

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